

Customer No.: 31561
Application No.: 10605,034
Docket No.: 10231-US-PA

IN THE CLAIMS

Claim 1. (Currently amended) A chip package structure process, comprising:

providing a matrix substrate;

disposing a plurality of chips on the matrix substrate and the chips are electrically connected to the matrix substrate;

disposing a stiffener on the matrix substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate, and wherein the stiffener has a plurality of openings and the chips are completely exposed by the openings of the stiffener;

providing a molding compound to cover the chips, the matrix substrate, the outer surface and the inner surface of the stiffener; and

dicing the molding compound, the matrix substrate and the stiffener to form a plurality of chip package structures.

Claim 2. (cancelled)

Claim 3. (original) The chip package structure process of claim 1, wherein the inner surface of the stiffener faces the chips.

Claim 4. (original) The chip package structure process of claim 1, wherein the stiffener is attached to the matrix substrate through an adhesive.

Claim 5. (original) The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate after dicing the molding compound, the matrix substrate and the stiffener.

Claim 6. (original) The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate before dicing the

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molding compound, the matrix substrate and the stiffener.

Claim 7. (original) The chip package structure process of claim 1, wherein the chips are attached to the matrix substrate through an adhesive in the step of disposing the plurality of chips and a plurality of wires are formed by wire-bonding to electrically connect the chips and the matrix substrate.

Claim 8. (original) The chip package structure process of claim 1, wherein a material of the stiffener is copper.

Claim 9. (currently amended) A chip package structure, comprising:

a substrate;

a chip, disposed on the substrate and electrically connected to the substrate;

a stiffener, disposed on the substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the substrate, and wherein the stiffener has at least an opening and the chip is completely exposed by the opening; and

a molding compound, covering the chips, the matrix substrate, the outer surface and the inner surface of the stiffener.

Claim 10. (cancelled)

Claim 11. (original) The chip package structure of claim 9, wherein the inner surface of the stiffener faces the chip.

Claim 12. (original) The chip package structure of claim 9, wherein the chip package structure further includes a plurality of wires and the chip disposed on the

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substrate is electrically connected to the substrate through the wires.

Claim 13. (original) The chip package structure of claim 9, wherein a material of the stiffener is copper.

Claim 14. (currently amended) A chip package structure, comprising:

a thin substrate, wherein the thin substrate has a thickness of between about 0.1mm --and about 0.5 mm;

a chip, disposed on the thin substrate and electrically connected to the thin substrate;

a stiffener, disposed on the thin substrate, and wherein the stiffener has at least an opening and the chip is completely exposed by the opening; and

a molding compound, covering the chips, the thin substrate and the stiffener.

Claim 15. (original) The chip package structure of claim 14, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the thin substrate and the molding compound covers the inner surface and the outer surface of the stiffener.

Claim 16. (original) The chip package structure of claim 14, wherein the inner surface of the stiffener faces the chip.

Claim 17. (cancelled)

Claim 18. (original) The chip package structure of claim 14, wherein the chip package structure further includes a plurality of wires and the chip disposed on the substrate is electrically connected to the substrate through the wires.

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